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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/009,248	01/20/98	OSAWA	K P972636

MM42/1028

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EXAMINER	
GRAYBILL, D	
ART UNIT	**PAPER NUMBER**
2814	7

DATE MAILED: 10/28/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)

1- File Copy

Office Action Summary

Application No.	Applicant(s)
09/009,248	Osawa et al.
Examiner	**Group Art Unit**
David E. Graybill	2814

☒ Responsive to communication(s) filed on *12 Aug 1999* .

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-9* is/are pending in the application.

Of the above, claim(s) *7-9* is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-6* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Applicant's election without traverse of Group II, claims 1-6 in Paper No. 6 is acknowledged. Claims 7-9 are withdrawn from further examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Takahashi (5198883) and Park (5847446).

Takahashi teaches:

1. A semiconductor device comprising: a semiconductor chip 50 having a plurality of electrode pads 54 formed at a periphery of a front surface thereof; a wiring film formed on a front surface side of said semiconductor chip by laminating an insulation film 57 on a lead pattern 42a; an outer connection terminal 51 formed so as to protrude above said wiring film; a plurality of leads 42a extending from said wiring film and connected to the electrode pads on said semiconductor chip at extended tip ends thereof; an external ring (ledge of pad 33 extending from and around the chip) provided so as to surround said semiconductor chip;

3. A lead frame comprising: a wiring film formed by laminating an insulation film 57 on a lead pattern 42a; an external connection terminal 51 formed so as to protrude above said wiring film; a plurality of leads 42a extending from said wiring film and forming connecting portions to electrode pads 54 on a semiconductor chip 50 at extended tip ends thereof; and an external ring (ledge of 33 extending from and around the chip) provided outside said wiring film;

5. An electronic apparatus including a printed wiring board loaded with a semiconductor chip, said semiconductor device comprising: a semiconductor chip 50 having a plurality of electrode pads 54 formed at a periphery of a front surface thereof; a wiring film 42a formed on a front surface side of said semiconductor chip by laminating an insulation film 57 on lead patterns; an outer connection terminal 51 formed so as to protrude above said wiring film; a plurality of leads 42a extending from said wiring film and connected to the electrode pads on said semiconductor chip at extended tip ends thereof; an external ring (ledge of 33 extending from and around the chip) provided so as to surround said semiconductor chip and a sealing resin 71 filled between said semiconductor chip and said external ring, wherein said external connection terminal and an electrode on said printed wiring board are connected.

However, Takahashi does not appear to explicitly teach:

An external ring formed with a plurality of through holes;

2. A semiconductor device according to Claim 1, further comprising an outwardly expanded open portion formed on an inner circumferential surface of said external ring and positioned on a rear surface side of said semiconductor chip;

An external ring having an opening portion capable of housing said semiconductor chip and formed with a plurality of through holes;

4. A lead frame according to Claim 3, further comprising an outwardly expanded open portion formed on an inner circumferential surface of said opening portion of said external ring and positioned on a rear surface side of said semiconductor chip;

6. An electronic apparatus according to Claim 5, further comprising an outwardly expanded open portion formed on an inner circumferential surface of said external ring and positioned on a rear surface side of said semiconductor chip.

Nonetheless, Park teaches:

An external ring (ledge of 120 extending from and around chip 110) formed with a plurality of through holes 124;

2. A semiconductor device according to Claim 1, further comprising an outwardly expanded open portion 124 formed on an inner circumferential surface of an external ring (ledge of 120 extending from and around chip 110) and positioned on a rear surface side of a semiconductor chip 110;

An external ring (ledge of 120 extending from and around chip 110) having an opening portion 124 capable of housing a semiconductor chip 120 and formed with a plurality of through holes 124;

4. A lead frame according to Claim 3, further comprising an outwardly expanded open portion 124 formed on an inner circumferential surface of an opening portion 124 of an external ring (ledge of 120 extending from and around chip 110) and positioned on a rear surface side of a semiconductor chip 110;

6. An electronic apparatus according to Claim 5, further comprising an outwardly expanded open portion 124 formed on an inner circumferential surface of an external ring (ledge of 120 extending from and around chip 110) and positioned on a rear surface side of a semiconductor chip 120.

Moreover, it would have been obvious to combine the invention of Park with the invention of Takahashi because it would increase package reliability.

The prior art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show processes of manufacturing a semiconductor package similar to the process of the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to the group receptionist at (703) 308-1782.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m..

The fax phone number for group 2800 is (703)305-3431.

David E. Graybill
Primary Examiner
Art Unit 2814

D.G.